FINFET WITH IMPROVED SEU PERFORMANCE

BACKGROUND

FinFETs (fin field effect transistors) are non-planar field effect transistors. A fin is a thin segment of semiconductor material standing on edge, thereby making available multiple surfaces for the formation of gate structures. The fins have first and second major surfaces that are opposite one another and usually are symmetric about a center plane that bisects the fin lengthwise. The major surfaces are often illustrated as being parallel as in U.S. Pat. No. 7,612,405 B2 or Pub. No. US2008/0128797 A1, which are incorporated herein by reference; but process limitations usually result in surfaces that slope outwardly from top to bottom of the fin with the result that the cross-section of the fin is trapezoidal in shape. In some cases, the two major surfaces meet at the top. In some embodiments, a separate gate structure may be located on each surface of each fin. In other embodiments, there is a common gate structure for all surfaces.

Doped source and drain regions are located on opposite sides of the gates. As in a planar FET, a voltage applied to the gate controls current flow in the channel that extends between the source and drain regions in the semiconductor beneath the gate.

Typically, finFETs are extremely small. Fin heights are usually on the order of tens of nanometers (nm.).

Unfortunately, the extremely small dimensions of typical finFET devices make the devices susceptible to single event upsets (SEUs) (sometimes also referred to as soft error upsets) and electronic noise signals. SEUs may be caused by radiation that generates electron-hole pairs at a sensitive node within a cell. The operation and performance of an integrated circuit may be substantially compromised by such SEUs. For example, field programmable gate arrays (FPGAs) and other programmable logic devices (PLDs) may be particularly sensitive to SEUs occurring in configuration random access memory (CRAM) cells. Other types of integrated circuits, such as microprocessors and application specific integrated circuits (ASICS), may also be sensitive to SEUs.

In addition, finFET devices are also susceptible to electronic noise signals which may be transmitted by way of conductive paths from other parts of an integrated circuit. In particular, substrate noise may adversely impact the performance of a finFET device used in an analog circuit application.

SUMMARY

In an illustrative embodiment, a finFET of the present invention comprises at least one fin, and typically several fins, with a trapping region in or on a substrate at the base of each fin. The trapping region traps some of the electrons or holes produced by radiation incident on the substrate. In a first illustrative embodiment, the trapping region is an implanted region having a conductivity type opposite that of the substrate. In a second illustrative embodiment, the trapping region is a defect region formed in the substrate at the base of the fin. In a third illustrative embodiment, the trapping region is an epitaxial region grown on the substrate.

In an illustrative embodiment, the finFET is formed by forming the fin or fins and then forming the trapping region at the base of the fin. Illustratively, the trapping region is formed by implanting in the substrate ions having a conductivity type opposite that of the substrate. Alternatively, the trapping region is formed by creating defects in the substrate at the base of one or more fins. Alternatively, the trapping region is formed by epitaxially growing on the substrate a region or regions having an opposite conductivity type to that of the substrate.

Numerous variations may be practiced in the illustrative embodiment.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and advantages of the present invention will be apparent to those of ordinary skill in the art in view of the following detailed description in which:

FIGS. **1**A, **1**B and **1**C are a prospective view, a plan view and a cross-sectional view of a first illustrative embodiment of the invention;

FIGS. **2**A and **2**B are a prospective view and a plan view of a second illustrative embodiment of the invention;

FIGS. **3**A and **3**B are a cross-sectional view and a plan view of a third illustrative embodiment of the invention;

FIG. **4** is a plan view of a layout in which the first, second, and third illustrative embodiments of the invention may be used;

FIG. **5** is a flow chart depicting an illustrative embodiment of the method of the invention;

FIGS. **6**A-**6**E are cross-sections depicting various stages in an illustrative implementation of the invention; and

FIGS. **7**A-**7**D are cross-sections depicting various stages in another illustrative implementation of the invention

DETAILED DESCRIPTION

FIGS. **1**A, **1**B, and **1**C are a prospective view, a plan view and a cross-sectional view of a first illustrative embodiment of the invention. As best shown in FIG. **1**A, finFET device **100** comprises a substrate **110** and a plurality of fins **120**, **130**, **140** extending upwards from the substrate. A gate structure **150** is formed on each fin with source and drain regions **122**, **124**; **132**, **134**; **142**, **144** on opposite sides of the gate. The fins are integral with the substrate and typically are formed by etching parallel channels in the substrate. This basic structure will be familiar to those skilled in the art.

In accordance with the invention, a trapping region **160** is formed in or on the substrate at the base of one or more of fins **120**, **130**, **140**. As shown in FIGS. **1**A-**1**C, one trapping region **160** extends along the substrate between the pair of adjacent fins **120**, **130**; and another trapping region **160** extends along the substrate between the pair of adjacent fins **130**, **140**. This arrangement, however, is only illustrative. More fins may be used; and as few as one fin may be used in the practice of the invention. Additional trapping regions may also be used such that there is a trapping region at the base on each side of each fin. And only a single trapping region can be used at the base of one of the fins. A field oxide region **170** is formed on top of each trapping region.

In the embodiment shown in FIGS. **1**A, **1**B and **1**C, the trapping regions are doped regions that are doped with ions having a conductivity type that is opposite to that of the conductivity type of the substrate. For example, if the conductivity type of the substrate is p-type, the trapping region is doped with an n-type dopant such as Arsenic. If the conductivity type of the substrate is n-type, the trapping region is doped with a p-type dopant such as Boron.

Advantageously, trapping regions **160** are coupled together and coupled directly or indirectly to a voltage source so as to reverse bias a p-n junction between the doped region of the trapping region and the oppositely-doped